

RFLM-501202LC-299

High Power Two Stage Passive Limiter Module

Features:

- High Peak Power Handling: +51 dBm
- High Average Power Handling: +36 dBm
- Low Insertion Loss: <0.4 dB
- Return Loss: >20 dB
- Low Flat Leakage Power : <21dBm
- Low Spike Energy Leakage: 0.2 ergs
- Recovery Time: 500 nsec
- Package: 8mm x 5mm x 2.5mm
- No external control lines or power supply required
- RoHS Compliant

Description:

The RFLM-501202LC-299 SMT Silicon PIN Diode Limiter Module offer both High Power CW and Peak Power protection in the 400 MHz to 2.5 GHz frequency range. It is based on a proven hybrid assembly technique utilized extensively in high reliability, mission critical applications. The RFLM-501202LC-299 offers excellent thermal characteristics in a compact, low profile 8mm x 5mm x 2.5mm package. The RFLM-501202LC-299 is designed for optimal small signal insertion loss permitting extremely low receiver noise figure while simultaneously offering excellent large input signal Flat Leakage for effective receiver protection in the 400 MHz to 2.5 GHz frequency range.

The limiter RF circuit characteristics provide outstanding passive receiver protection (always on) which protects against High Average Power up to 36dBm, High Peak Power up to 51 dBm pulsed (pulse width = 1 usec, duty cycle = 0.1%), maintains low flat leakage to less than 20dBm (typical), and reduces Spike Leakage to less than 0.2 ergs.

ESD and Moisture Sensitivity Rating

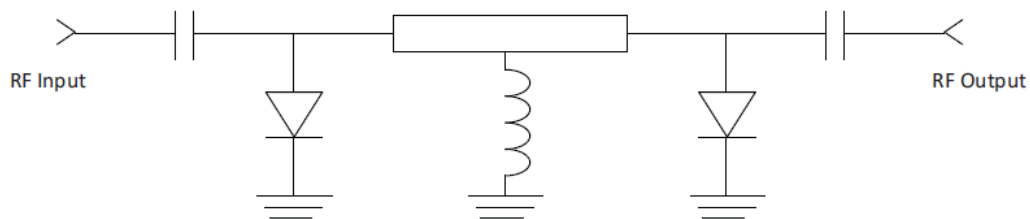
The RFLM501202LC-299 Limiter Module carries a Class 1C ESD rating (HBM) and an MSL 1 moisture rating.

Thermal Management Features

The RFLM-501202LC-299 based substrate has been design to offer superior long term reliability in the customer's application by utilizing ultra-thin Au plating to combat Au embrittlement concerns. Also, a proprietary design methodology has minimized the thermal resistance from the PIN Diode junction to base. The two stage limiter design employs a second stage limiter and quarter wavelength spacer detector circuit which permits ultra-fast turn on of the High Power PIN Diodes. This circuit topology couple with the thermal characteristic of the

substrate design enables reliably handling High Input RF Power up to 36dBmCW and RF Peak Power levels up to 51dBm(1 uSec pulse width @ 0.1% duty cycle with base plate temperature at 85°C).

RFLM-501202LC-299 Limiter Module Equivalent Schematic



Absolute Maximum Ratings

@ $Z_0=50\Omega$, $T_A=+25^\circ\text{C}$ as measured on the base ground surface of the device.

Parameter	Conditions	Absolute Maximum Value
Operating Temperature		-65°C to 125°C
Storage Temperature		-65°C to 150°C
Junction Temperature		175°C
Assembly Temperature	$T = 30$ seconds	260°C
RF Peak Incident Power	$T_{\text{CASE}}=85^\circ\text{C}$, source and load $\text{VSWR} < 1.2$, RF Pulse width = 1 uSec, duty cycle = 0.1%, derated linearly to 0 W at $T_{\text{CASE}}=150^\circ\text{C}$ (See note 1)	52 dBm
RF CW Incident Power		37 dBm
Assembly Temperature		260°C for 30 seconds

Note 1: T_{CASE} is defined as the temperature of the bottom ground surface of the device.

RFLM501202LC-299 Electrical Specifications

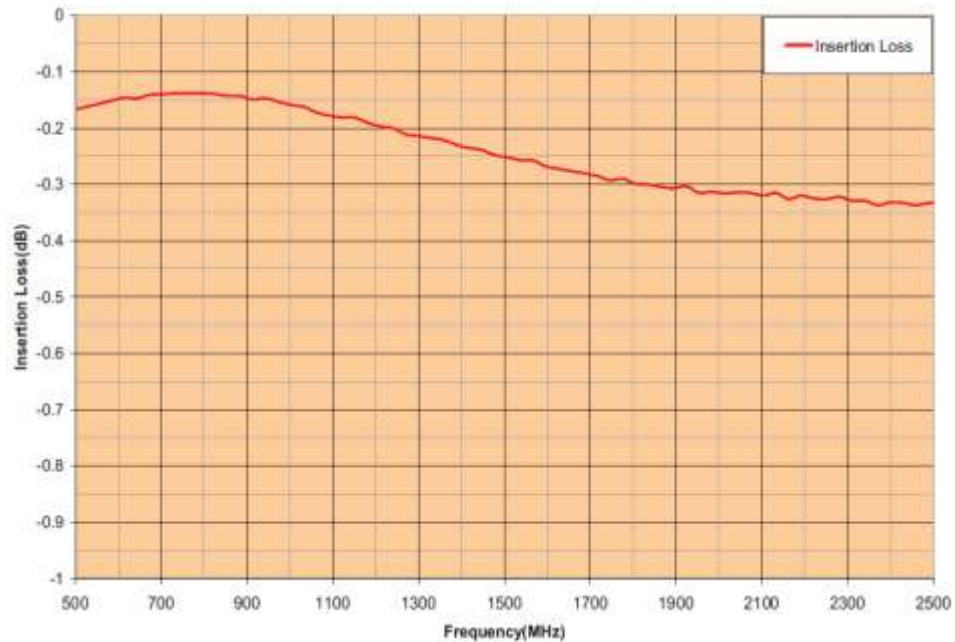
@ $Z_0=50\Omega$, $T_A=+25^\circ\text{C}$ as measured on the base ground surface of the device.

Parameters	Symbol	Test Conditions	Min Value	Typ Value	Max Value	Units
Frequency	F		0.4		2.5	GHz
Insertion Loss	IL	$400\text{ MHz} \leq F \leq 2.5\text{ GHz}$, $P_{in}=0\text{ dBm}$		0.4	0.6	dB
Insertion Loss Rate of Change vs Operating Temperature	ΔIL	$400\text{ MHz} \leq F \leq 2.5\text{ GHz}$, $P_{in} \leq -10\text{ dBm}$		0.005		dB/ $^\circ\text{C}$
Return Loss	RL	$400\text{ MHz} \leq F \leq 2.5\text{ GHz}$, $P_{in}=0\text{ dBm}$	18	20		dB
Input 1 dB Compression Point	IP_{1dB}	$400\text{ MHz} \leq F \leq 2.5\text{ GHz}$		8		dBm
2 nd Harmonic	$2F_0$	$P_{in}=0\text{ dBm}$, $F_0=2.0\text{ GHz}$		-50	-45	dBc
Peak Incident Power	$P_{inc(PK)}$	RF Pulse = 1 usec, duty cycle = 0.1%, $t_{rise} \leq 2\text{ us}$, $t_{fall} \leq 2\text{ usec}$		51	52	dBm
CW Incident Power	$P_{inc(CW)}$	$400\text{ MHz} \leq F \leq 2.5\text{ GHz}$		36	37	dBm
Flat Leakage	FL	$P_{in}=50\text{ dBm}$, RF Pulse width = 1 us, duty cycle = 0.1%, $t_{rise} \leq 2\text{ us}$, $t_{fall} \leq 2\text{ us}$		21	23	dBm
Spike Leakage	SL	$P_{in}=50\text{ dBm}$, RF Pulse width = 1 us, duty cycle = 0.1%		0.2	0.3	erg
Recovery Time	T_R	50% falling edge of RF Pulse to 1 dB IL, $P_{in}=50\text{ dBm}$ peak, RF PW = 1 us, duty cycle = 0.1%, $t_{rise} \leq 2\text{ us}$, $t_{fall} \leq 1\text{ usec}$		500	750	nsec

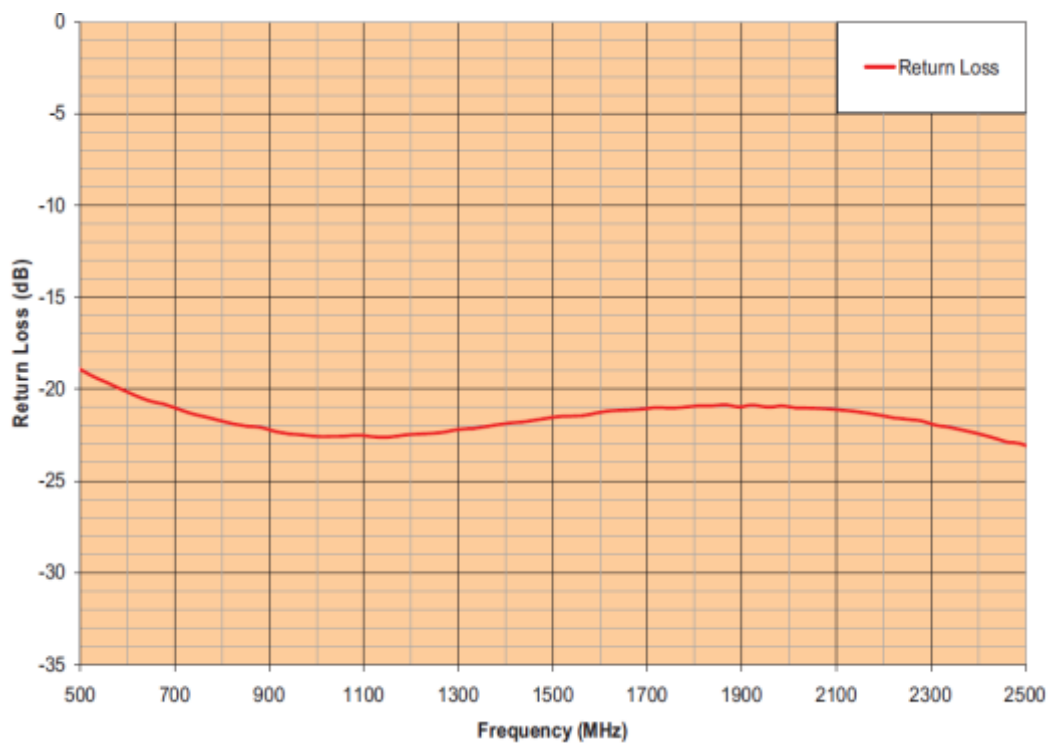
RFLM-501202LC-299 Typical Performance

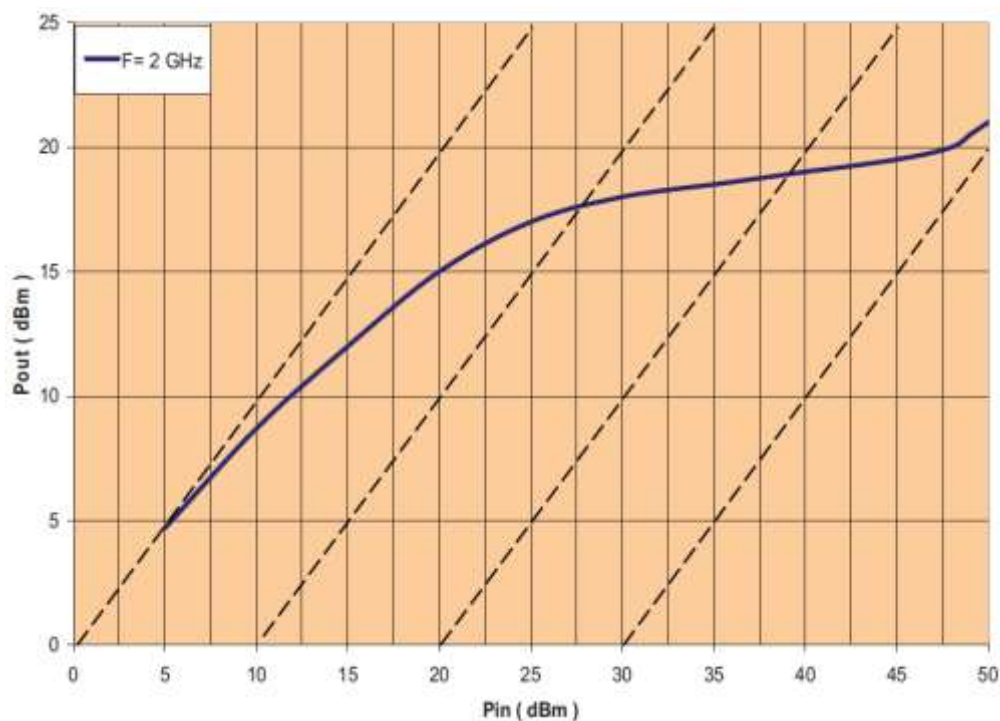
$Z_0 = 50\Omega$, $T_{CASE} = 25^\circ\text{C}$, $PIN = -20\text{ dBm}$ as measured on the Ground Plane of the device.

RFLM-501202LC-299 Insertion Loss vs Frequency



RFLM-501202LC-299 Return Loss vs Frequency



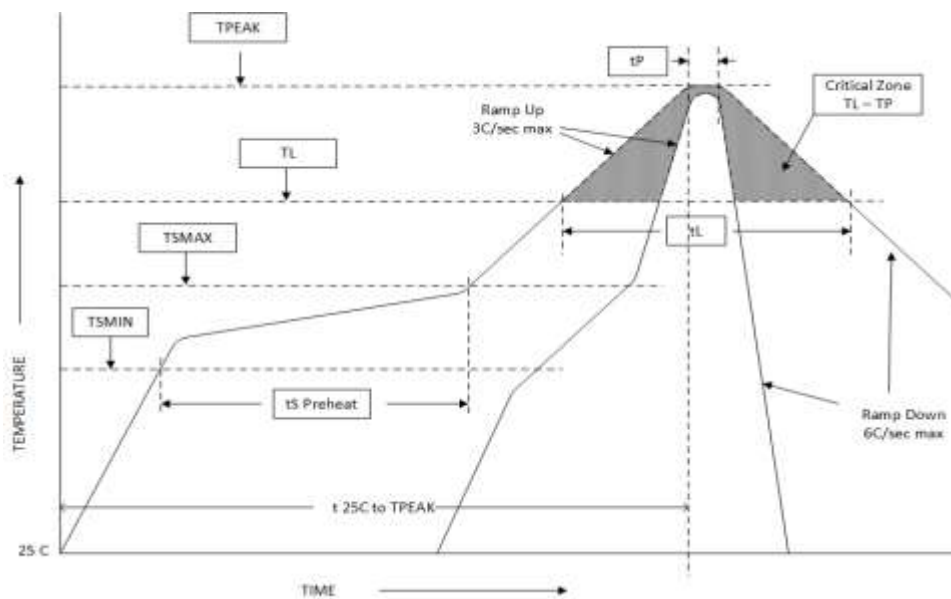
RFLM-501202LC-299 Flat Leakage: Peak Power P_{out} vs P_{in} 

Assembly Instructions

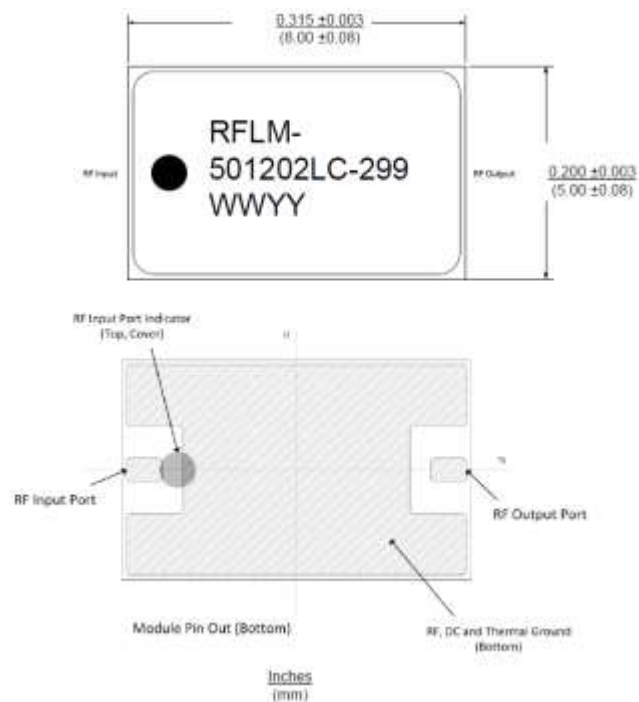
The RFLM-501202LC-299 may be attached to the printed circuit card using solder reflow procedures using either RoHS or Sn63/ Pb37 type solders per the Table and Temperature Profile Graph shown below:

Profile Parameter	Sn-Pb Assembly Technique	RoHS Assembly Technique
Average ramp-up rate (T_L to T_P)	3°C/sec (max)	3°C/sec (max)
Preheat		
Temp Min (T_{smin})	100°C	100°C
Temp Max (T_{smax})	150°C	150°C
Time (min to max) (t_s)	60 – 120 sec	60 – 120 sec
T_{smax} to T_L		
Ramp up Rate		3°C/sec (max)
Peak Temp (T_P)	225°C +0°C / -5°C	245°C +0°C / -5°C
Time within 5°C of Actual Peak Temp (T_P)	10 to 30 sec	20 to 40 sec
Time Maintained Above:		
Temp (T_L)	183°C	217°C
Time (t_L)	60 to 150 sec	60 to 150 sec
Ramp Down Rate	6°C/sec (max)	6°C/sec (max)
Time 25°C to T_P	6 minutes (max)	8 minutes (max)

Solder Re-Flow Time-Temperature Profile



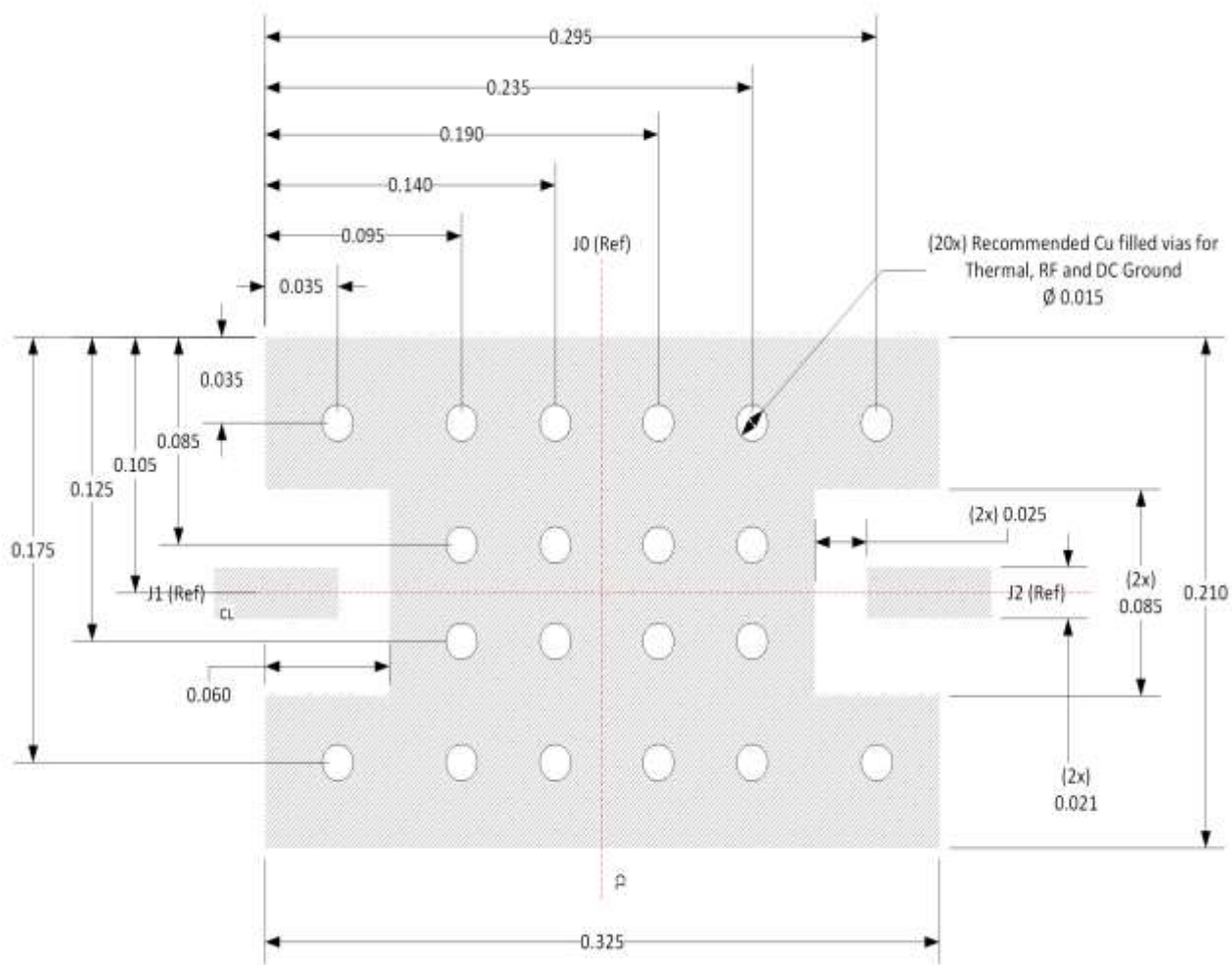
RFLM-501202LC-299 Limiter Module Package Outline Drawing



Notes:

- 1) Metalized area on backside is the RF, DC and Thermal ground. In user's end application this surface temperature must be managed to meet the power handling requirements.
- 2) Back side metallization is thin Au termination plating to combat Au embrittlement (15 u in typ Au plated over Ti-Pd).

Recommended RF Circuit Solder Footprint for the RFLM501202LC-299



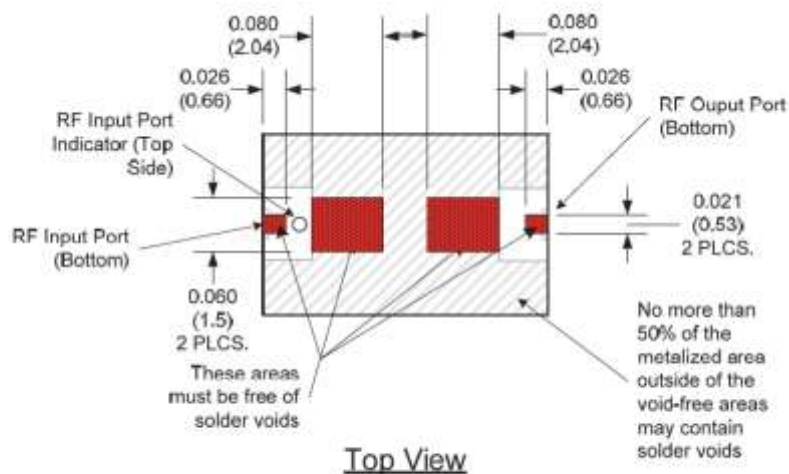
Notes:

- 1) Recommended PCB material is rogers 4350, 10 mils thick.
- 2) Hatched area is RF, DC and Thermal Ground. Vias should be solid Cu filled and Au plated for optimal heat transfer from backside of Limiter Module through circuit vias to thermal ground.

Thermal Design Considerations:

The design of the RFLM-501202LC-299 Limiter Module permits the maximum efficiency in thermal management of the PIN Diodes while maintaining extremely high reliability. Optimum Limiter performance and reliability of the device can be achieved by the maintaining the base ground surface temperature of less than 85°C.

There must be a minimal thermal and electrical resistance between the limiter and ground. Adequate thermal management is required to maintain a T_{jc} at less than $+175^{\circ}\text{C}$ and to avoid adversely affecting the semiconductor reliability. Special care must be taken to assure that minimal voiding occurs in the solder connection in the areas shaded in red in the figure shown below:



Dimensions in inches (mm).

Part Number Ordering Detail:

The RFLM-501202LC-299 Limiter Module is available in the following format.

Part Number	Description	Packaging
RFLM-501202LC-299	400 MHz to 2.5 GHz Band Limiter	Gel-Pack